LED Driver

W2RG012RN

OMRON

■ Features

Optimal IC for LED performance control

- The built-in exponential PWM gradation control function with up to 256 levels enables visually pleasing fade-ins and fade-outs.
- Capable of dynamically driving matrix-connected LEDs and individually controlling up to 128 channels.
- Serial bus connection allows up to 15 of these ICs to be connected on the same communication line.
- 24 constant current outputs are housed in a compact package with 7 x 7 mm dimensions.
- Built-in thermal shutdown

■ Model Number Legend

W2R G012RN (1) IC
(1) (2) (2) Series name

■ Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Target terminals
Power supply voltage	VDD	-0.3 to 7.0	V	VDD
Input voltage	VIN	-0.3 to VDD + 0.3 ≤ 7.0	V	SDA, SCL, $\overline{RST}$, $\overline{CE}$, ADR1, ADR0, DIV, COM
Signal output voltage	VSOUT	-0.3 to VDD + 0.3 ≤ 7.0	V	SDO, OUTDC
Drive output voltage	VDOUT	-0.3 to 20	V	OUT0R to 7R, OUT0G to 7G, OUT0B to 7B, OUTS0 to S3
Drive output current/pin	IDOUT	80 (*1)	mA	OUT0R to 7R, OUT0G to 7G, OUT0B to 7B
Switching output current/pin	IDOUTS	20	mA	OUTS0 to S3
Allowable loss	Pd1	3.43 (*2)	W	-
	Pd2	1.80 (*2)	W	-
	Pd3	1.16 (*2)	W	-
Operating ambient temperature	Topr	-20 to 85	°C	-
Storage ambient temperature	Tstg	-40 to 150	°C	-

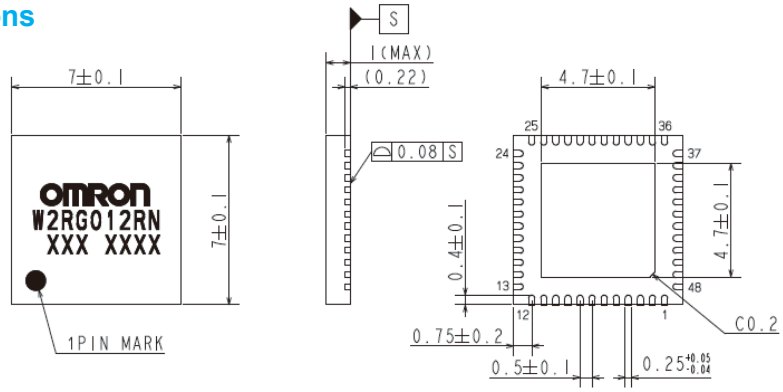
*1. Consider the power consumption and allowable loss before use.
*2. Values when a standard board (70 mm x 70 mm x 1.6 mmt, FR-4) is mounted. When used at a temperature of Ta=25°C or higher, reduce by the temperature derating factor Rtd [mW/°C].
Pd1: Rtd = 27.4 mW/°C for a double-sided board with a copper foil area of 4900 mm² on the backside.
Pd2: Rtd = 14.4 mW/°C for a double-sided board with a copper foil area of 225 mm² on the backside.
Pd3: Rtd = 9.28 mW/°C for a single-sided board with a copper foil area of 36 mm².

■ Recommended Operating Conditions

Item	Symbol	Rating	Unit	Target terminals
Power supply voltage	VDD	3.0 to 5.5	V	VDD
Input voltage	VIN	0 to VDD	V	SDA, SCL, $\overline{RST}$, $\overline{CE}$, ADR1, ADR0, DIV, COM
Signal output current	ISOUT	-10 to 10	mA	SDO, OUTDC
Communication clock frequency	fSCL	Max.5 (*1)	MHz	SCL

*1. Consider the timing characteristics before use.

■ External Dimensions



[Unit: mm]

■ Electrical Characteristics

(1) DC characteristics

(Ta = 25°C, VDD = 5V)

Item	Symbol	Conditions	Standard values			Unit	Target terminals
			Min.	Typ.	Max.		
High level input voltage	VIH	-	VDD × 0.7	-	-	V	SDA, SCL, $\overline{RST}$, $\overline{CE}$
Low level input voltage	VIL	-	-	-	VDD × 0.3	V	
A/D input voltage	VAD1	"10" output	VDD × 0.9	-	VDD + 0.3	V	ADR1, ADR0, DIV, COM
	VAD2	"11" output	VDD × 0.6	-	VDD × 0.7	V	
	VAD3	"01" output	VDD × 0.3	-	VDD × 0.4	V	
	VAD4	"00" output	-0.3	-	VDD × 0.1	V	
High level signal output voltage	VSOH	ISOUT = -5 mA	VDD - 0.5	-	-	V	SDO, OUTDC
Low level signal output voltage	VSOL	ISOUT = 5 mA	-	-	0.5	V	
On-resistance 1	RON1	-	-	6.3	10	Ω	OUT0R to 7R, OUT0G to 7G, OUT0B to 7B,
Pin-to-pin current accuracy	ΔIP	IDOUT = 20 mA	-3	-	+3	%	
Inter-device current accuracy	ΔID	IDOUT = 20 mA	-6	-	+6	%	
Drive output leakage current	IDL	-	-	-	1	μA	
On-resistance 2	RON2	-	-	9.0	20	Ω	OUTS0 to S3
Current consumption during operation	IDD	Total output: IDOUT = 20 mA	-	5.0	7.0	mA	VDD

(2) Timing characteristics

(2)-1 Addressed serial communication

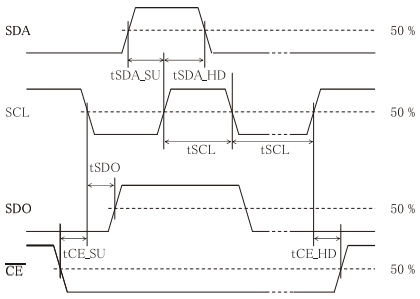
(Ta = -20 to 85°C, VDD = 3.0 to 5.5V)

Item	Symbol	Conditions	Standard values			Unit	Target terminals
			Min.	Typ.	Max.		
Communication clock pulse width	tSCL	-	100	-	-	ns	SCL
Data setup time	tSDA_SU	-	90	-	-	ns	SCL, SDA
Data hold time	tSDA_HD	-	90	-	-	ns	
$\overline{CE}$ setup time	tCE_SU	-	50	-	-	ns	SCL, SDA, $\overline{CE}$
$\overline{CE}$ hold time	tCE_HD	-	50	-	-	ns	
Data output time	tSDO	Load capacitance 100 pF	-	-	80	ns	SCL, SDO

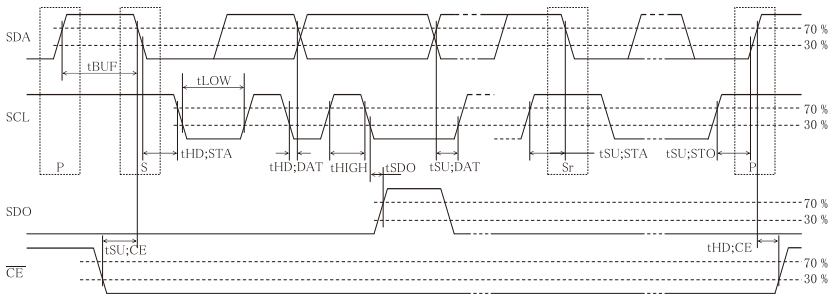
(2)-2 I2C-compliant serial communication

(Ta = -20 to 85°C, VDD = 3.0 to 5.5V)

Item	Symbol	Conditions	Standard values			Unit	Target terminals
			Min.	Typ.	Max.		
Clock "L" period	tLOW	-	50	-	-	ns	SCL
Clock "H" period	tHIGH	-	50	-	-	ns	
Bus release time	tBUF	-	80	-	-	ns	SDA
Start setup time	tSU;STA	-	50	-	-	ns	SCL, SDA
Start hold time	tHD;STA	-	50	-	-	ns	
Stop setup time	tSU;STO	-	50	-	-	ns	
Data setup time	tSU;DAT	-	30	-	-	ns	
Data hold time	tHD;DAT	-	0	-	-	ns	
$\overline{CE}$ setup time	tSU;CE	-	50	-	-	ns	SCL, SDA, $\overline{CE}$
$\overline{CE}$ hold time	tHD;CE	-	50	-	-	ns	
Data output time	tSDO	Load capacitance 100 pF	-	-	80	ns	SCL, SDO



Addressed serial communication



I2C-compliant serial communication

■ Function Overview

24 channels of LEDs are driven by constant current or constant voltage.
Furthermore, dynamic lighting (pulsed lighting) of LEDs connected in a matrix can be performed. During dynamic lighting, the LEDs of 48 channels (2-segment), 96 channels (4-segment), and 128 channels (8-segment) can be individually gradation-controlled.

(1) Command reception
The LED lighting command is received via serial communication. In terms of communication methods, three types of addressed serial communication and I2C-compliant serial communication are supported.
Up to 128 LED lighting data can be sent continuously. The start signal and device address only need to be specified once, thus reducing the overall communication volume.

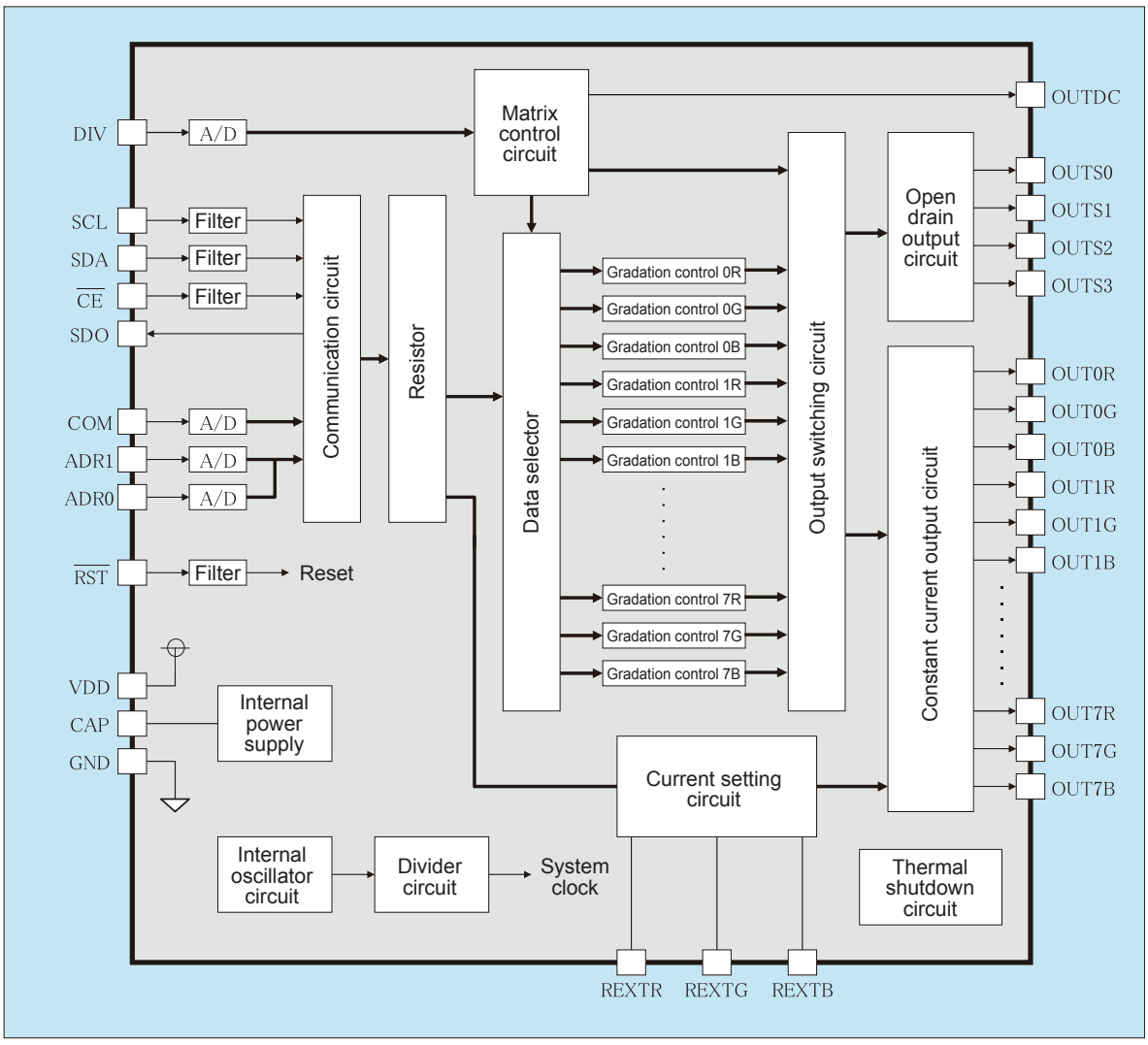
(2) Gradation control
256 gradation levels can be illuminated. Each gradation level is assigned to a duty ratio according to an exponential function, allowing expression that corresponds to the characteristics of human vision.

(3) Matrix control
It supports matrix connections of 24 x 1, 24 x 2, 24 x 4, and 16 x 8.
By controlling the switching timing of dynamic lighting, accidental lighting during switching can be prevented.

(4) Power-saving control
Drives the power consumption during LED lighting at 75%/50%/25% of the normal operating power. Batch switching is possible using communication commands, making it easy to switch between normal and power-saving modes.
The control method can be selected between current control and duty ratio control.
Current control switches the output current to 75%, 50%, or 25% based on the current set at the current setting terminals REXTR/REXTG/REXTB. Duty ratio control switches the output duty ratio to 75%, 50%, or 25% based on the gradation-specified duty ratio.

(5) Number of control channels
Up to 15 devices can be connected by specifying the address. This allows for the control of up to 1920 channels of LEDs. In addition, more devices can be connected by switching $\overline{CE}$ terminals.

■ Block Diagram



■ Terminal List

No.	Terminal name	Terminal description	I/O	Function
1	SDA	Serial data input	I	CMOS, Filter
2	SCL	Serial clock input	I	CMOS, Filter
3	$\overline{CE}$	Chip enable input (*1)	I	CMOS, Filter
4	VDD	Power supply	P	
5	CAP	Capacitor (*2)	—	
6	GND	Ground	P	
7	ADR1	Device address 1	I	Resistance voltage divider input
8	ADR0	Device address 0	I	Resistance voltage divider input
9	DIV	Division mode	I	Resistance voltage divider input
10	COM	Communication mode	I	Resistance voltage divider input
11	REXTR	Current setting resistor R	—	
12	REXTG	Current setting resistor G	—	
13	REXTB	Current setting resistor B	—	
14	OUT0R	Output 0R	O	Constant current
15	OUT0G	Output 0G	O	Constant current
16	OUT0B	Output 0B	O	Constant current
17	GND	Ground	P	
18	OUT1R	Output 1R	O	Constant current
19	OUT1G	Output 1G	O	Constant current
20	OUT1B	Output 1B	O	Constant current
21	OUT2R	Output 2R	O	Constant current
22	OUT2G	Output 2G	O	Constant current
23	GND	Ground	P	
24	OUT2B	Output 2B	O	Constant current

No.	Terminal name	Terminal description	I/O	Function
25	OUT3R	Output 3R	O	Constant current
26	OUT3G	Output 3G	O	Constant current
27	OUT3B	Output 3B	O	Constant current
28	OUT4R	Output 4R	O	Constant current
29	OUT4G	Output 4G	O	Constant current
30	OUT4B	Output 4B	O	Constant current
31	GND	Ground	P	
32	OUT5R	Output 5R	O	Constant current
33	OUT5G	Output 5G	O	Constant current
34	OUT5B	Output 5B	O	Constant current
35	OUT6R	Output 6R	O	Constant current
36	OUT6G	Output 6G	O	Constant current
37	GND	Ground	P	
38	OUT6B	Output 6B/Output switching 4	O	Constant current
39	OUT7R	Output 7R/Output switching 5	O	Constant current
40	OUT7G	Output 7G/Output switching 6	O	Constant current
41	OUT7B	Output 7B/Output switching 7	O	Constant current
42	OUTS0	Output switching 0	O	N-ch open drain
43	OUTS1	Output switching 1	O	N-ch open drain
44	OUTS2	Output switching 2	O	N-ch open drain
45	OUTS3	Output switching 3	O	N-ch open drain
46	OUTDC	Synchronization control output	O	CMOS
47	SDO	Serial data output	O	CMOS
48	$\overline{RST}$	Reset (*3)	I	CMOS, Filter, Pull-up

*1. If the $\overline{CE}$ terminal is not used, set it to low (L). (Excluding CE-D8 mode)
*2. The CAP terminal connects a power supply smoothing capacitor. Connect a 0.1 μF capacitor between the CAP terminal and GND.
*3. The $\overline{RST}$ terminal has a built-in 100 kΩ pull-up resistor. If not used, we recommend connecting a 0.1 uF capacitor between the $\overline{RST}$ terminal and GND for stable operation.
*4. Put unused output terminals in the open state.

■ Terminal Description

(1) ADR terminal
Set the device address by inputting the resistance voltage divider. Table 1 shows the correspondence between device addresses and ADR pin voltages.

(2) DIV terminal
Set the matrix configuration of the LEDs to be connected by inputting the DIV terminal resistance voltage divider.
Table 2 shows the correspondence between matrix configurations and DIV terminal voltages, and Table 3 shows the correspondence between matrix configurations and terminal functions.

(3) COM terminal
Set the communication mode by inputting the the resistance voltage divider. Table 4 shows the correspondence between communication modes and COM pin voltages.

(4) REXT terminal
The current is set by connecting to GND via an external REXT resistor. Table 5 shows the current vs. REXT resistor.

(5) $\overline{RST}$ terminal
When the input is “L” , each buffer is in the initial state, the constant-current output terminal and the open-drain output terminal are in open outputs, and the CMOS output terminal is in “L” output.

Table 1: Device address and ADR terminal voltage

Device address	ADR1	ADR0
0000	GND	GND
0001	GND	VDD×1/3
0010	GND	VDD
0011	GND	VDD×2/3
0100	VDD×1/3	GND
0101	VDD×1/3	VDD×1/3
0110	VDD×1/3	VDD
0111	VDD×1/3	VDD×2/3
1000	VDD	GND
1001	VDD	VDD×1/3
1010	VDD	VDD
1011	VDD	VDD×2/3
1100	VDD×2/3	GND
1101	VDD×2/3	VDD×1/3
1110	VDD×2/3	VDD
1111(reserve)	VDD×2/3	VDD×2/3

Table 2: Matrix configuration and DIV terminal voltage

Matrix configuration	DIV
24×1	GND
24×2	VDD×1/3
24×4	VDD
16×8	VDD×2/3

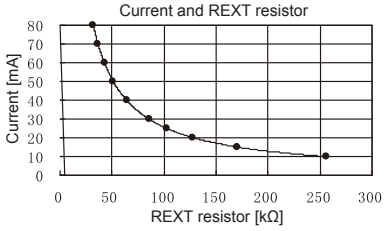
Table 3: Matrix configuration and terminal voltage

Output terminal	Matrix configuration			
	24×1	24×2	24×4	16×8
OUT0R	OUT0R			
OUT0G	OUT0G			
OUT0B	OUT0B			
OUT1R	OUT1R			
OUT1G	OUT1G			
OUT1B	OUT1B			
OUT2R	OUT2R			
OUT2G	OUT2G			
OUT2B	OUT2B			
OUT3R	OUT3R			
OUT3G	OUT3G			
OUT3B	OUT3B			
OUT4R	OUT4R			
OUT4G	OUT4G			
OUT4B	OUT4B			
OUT5R	OUT5R			
OUT5G	OUT5G			(Not used)
OUT5B	OUT5B			(Not used)
OUT6R	OUT6R			(Not used)
OUT6G	OUT6G			(Not used)
OUT6B	OUT6B			OUTS4
OUT7R	OUT7R			OUTS5
OUT7G	OUT7G			OUTS6
OUT7B	OUT7B			OUTS7
OUTS0	OUTS0			
OUTS1	(Not used)	OUTS1		
OUTS2	(Not used)	(Not used)	OUTS2	
OUTS3	(Not used)	(Not used)	OUTS3	

Table 4 shows the correspondence between communication modes and COM pin voltages.

Communication mode	COM
Addressed serial communication (SP-D8)	GND
Addressed serial communication (SP-D7)	VDD×1/3
I2C-compliant serial communication (I2C)	VDD
Addressed serial communication (CE-D8)	VDD×2/3

Table 5: Current and the REXT resistor



Current [mA]	REXT resistor [kΩ]
10	256
15	171
20	128
25	102
30	85.3
40	64.0
50	51.2
60	42.7
70	36.6
80	32.0

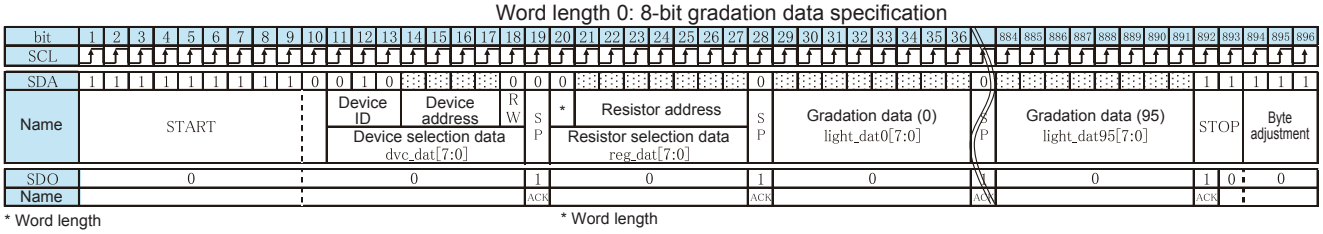
(Current setting method)
IDOUT [mA] = 2560/REXT resistor [kΩ]
(Recommended operating range)
IDOUT: 10 to 80 mA (Instantaneous value)
*1. The effective value is IDOUT/division factor.

■ Communication Specifications

This IC supports four communication methods. Set at the communication mode setting terminal (COM).

(1) Addressed serial communication method (SP-D8 mode)

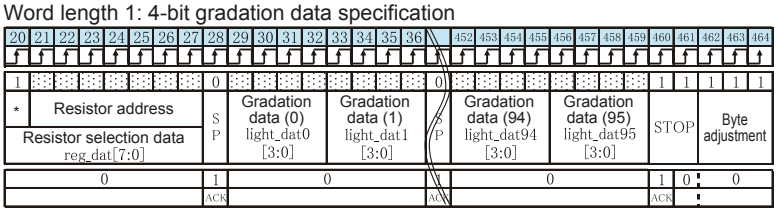
Word length 0: 8-bit gradation data specification



* Word length

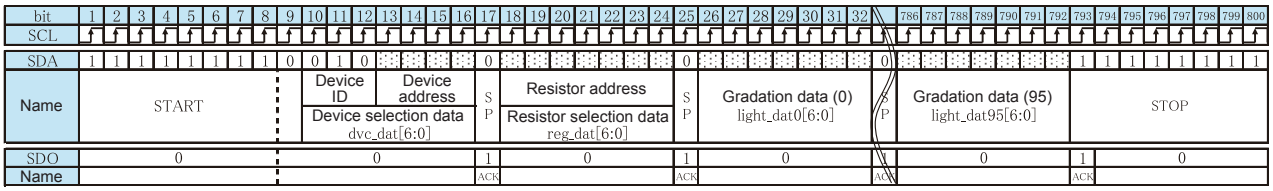
* Word length

Word length 1: 4-bit gradation data specification



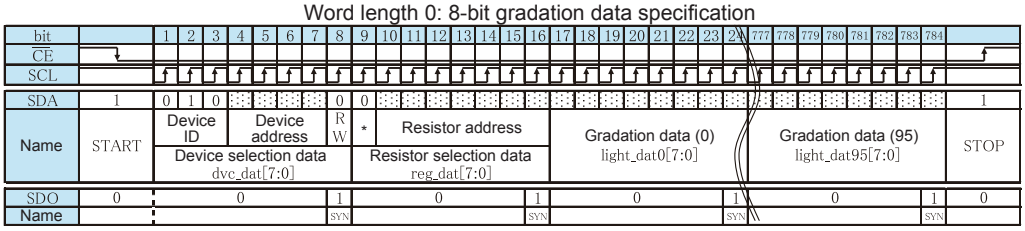
Byte adjustment: When sending data in 8-bit units, specify “1” for the remainder pit after STOP.

(2) Addressed serial communication method (SP-D7 mode)



(3) Addressed serial communication method (CE-D8 mode)

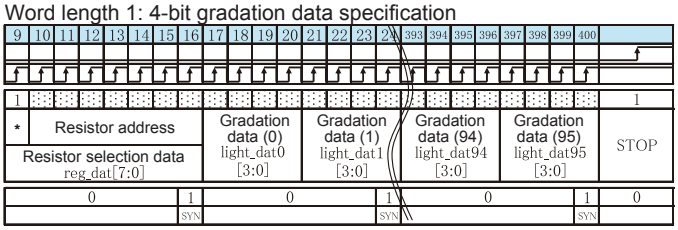
Word length 0: 8-bit gradation data specification



* Word length

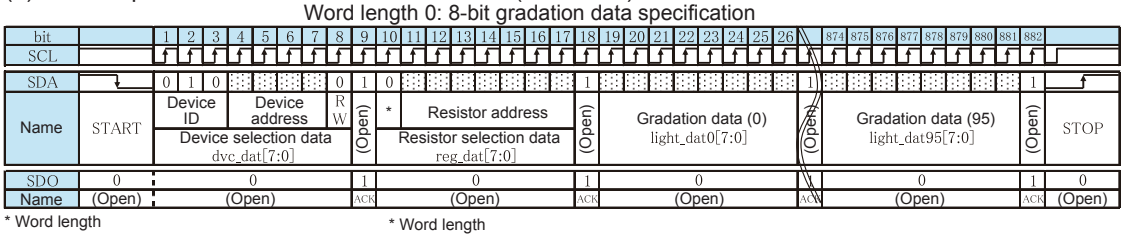
* Word length

Word length 1: 4-bit gradation data specification



(4) I2C-compliant serial communication method (I2C mode)

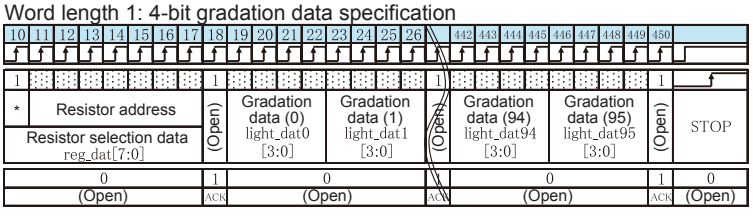
Word length 0: 8-bit gradation data specification



* Word length

* Word length

Word length 1: 4-bit gradation data specification



The names and communication formats of each communication method are shown below.

Communication mode name	Abbreviation start signal	Start signal	Stop signal	Separator	Data width	Response
Addressed serial communication method (SP-D8 mode)	SP-D8	"1 1111 1111 0"	"1 1111 1111"	0: Continue 1: End	8	ACK (NACK)
Addressed serial communication method (SP-D7 mode)	SP-D7	"1111 1111 0"	"1111 1111"	0: Continue 1: End	7	ACK (NACK)
Addressed serial communication method (CE-D8 mode)	CE-D8	$\overline{CE}$ falling edge	$\overline{CE}$ rising edge	(None)	8	SYN
I2C-compliant serial communication (I2C mode)	I2C	I2C standard compliant	I2C standard compliant	I2C standard compliant	8	ACK (NACK)

[Start signal] Regardless of whether in standby or in communication, communication is initialized and the device is placed in a state waiting for device selection data.

[Stop signal] Terminates communication and enters a start signal waiting state.
With SP-D8/SP-D7, the communication termination procedure (sending "1" to the separator / sending stop signal) can be omitted by sending the start signal after sending the gradation data.

[Separator] A bit to be inserted between transmitted data.
With SP-D8/SP-D7, sending "1" to the separator terminates communication and enters the state of waiting for a stop signal or start signal.
With I2C, the separator is assigned to the ACK response.

[Data width] Transmission data bit width.
With SP-D7, the data that can be specified is limited (no word length specification, 128 gradation specification).

[Response] Response type. At the falling edge of the SCL signal, this IC outputs data to the SDO terminal.
With SP-D8/SP-D7/I2C, the received data is checked and the result is returned (ACK or NACK).
With CE-D8, a synchronous signal is output to indicate that communication is in progress (SYN).
The received data is not checked.

The command structure is shown below.

[Device specification]

Received data is captured when the device ID and device address match the IC settings. The device ID is fixed as "010" . The same command can be sent to all devices by specifying "1111" as the device address. The correspondence between device addresses and device address terminals is shown in the table below.

Communication mode	Device selection data dvc_dat[7:0]							
	7	6	5	4	3	2	1	0
	Device ID			Device address				RW
Standard	0	1	0	ADR1[1:0]		ADR0[1:0]		0
SP-D7								—

[Resistor specification]

Communication mode	Device selection data reg dat[7:0]							
	7	6	5	4	3	2	1	0
Standard	*	Resistor address						
SP-D7	—							

* Word length

1. Word length
Specify the data unit for gradation data.

Word length specification	Word length
"0"	8bit
"1"	4bit

2. Register address (lighting position specification)
Specify the address of the gradation register. The upper limit of addresses that can be specified and the number of gradation data that can be continuously transferred vary depending on the division mode setting and word length specification (Table 6).

3. Resistor address (special address)
By specifying 0x7F (127), all gradation registers can be specified in one batch.
By specifying 0x78 (120), the power-saving data register can be specified.

[Gradation data]

Communication mode	Device selection data light_dat[7:0]							
	7	6	5	4	3	2	1	0
Standard (8 bits)	Gradation data							
Standard (4 bits)	Gradation data N				Gradation data N+1			
SP-D7	Gradation data							—

1. Gradation specification
Specify the gradation data in one of the following formats: 8-bit (256 gradations), 7-bit (128 gradations), or 4-bit (16 gradations). (Table 7)

2. Power-saving mode
When specifying the power-saving data register in the register address, the lower 4 bits are treated as power-saving data.

Power-saving data	Output current or output duty cycle
"00"	100 %
"01"	75 %
"10"	50 %
"11"	25 %

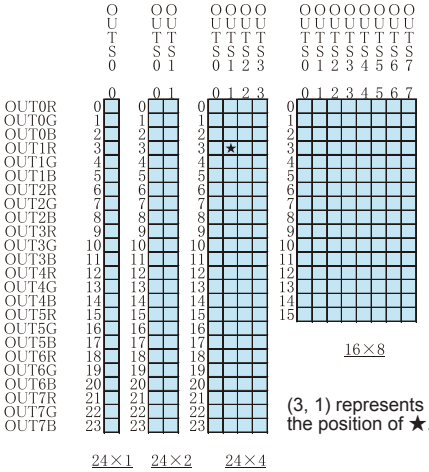
Communication mode	Device selection data light_dat[7:0]							
	7	6	5	4	3	2	1	0
Standard	0	0	0	0	Power-saving data (current control)		Power-saving data (duty cycle control)	
SP-D7	—	0	0	0				

Table 6: Register address and lighting position

Resistor address	Matrix configuration				
	24×1	24×2	24×4	16×8	
				Even columns	Odd columns
0x00 (0)	(0, 0)	(0, 0)	(0, 0)	(0, 0)	(1, 0)
0x01 (1)	(1, 0)	(1, 0)	(1, 0)	(2, 0)	(3, 0)
0x02 (2)	(2, 0)	(2, 0)	(2, 0)	(4, 0)	(5, 0)
0x03 (3)	(3, 0)	(3, 0)	(3, 0)	(6, 0)	(7, 0)
0x04 (4)	(4, 0)	(4, 0)	(4, 0)	(8, 0)	(9, 0)
0x05 (5)	(5, 0)	(5, 0)	(5, 0)	(10, 0)	(11, 0)
0x06 (6)	(6, 0)	(6, 0)	(6, 0)	(12, 0)	(13, 0)
0x07 (7)	(7, 0)	(7, 0)	(7, 0)	(14, 0)	(15, 0)
0x08 (8)	(8, 0)	(8, 0)	(8, 0)	(0, 1)	(1, 1)
0x09 (9)	(9, 0)	(9, 0)	(9, 0)	(2, 1)	(3, 1)
0x0A (10)	(10, 0)	(10, 0)	(10, 0)	(4, 1)	(5, 1)
0x0B (11)	(11, 0)	(11, 0)	(11, 0)	(6, 1)	(7, 1)
0x0C (12)	(12, 0)	(12, 0)	(12, 0)	(8, 1)	(9, 1)
0x0D (13)	(13, 0)	(13, 0)	(13, 0)	(10, 1)	(11, 1)
0x0E (14)	(14, 0)	(14, 0)	(14, 0)	(12, 1)	(13, 1)
0x0F (15)	(15, 0)	(15, 0)	(15, 0)	(14, 1)	(15, 1)
0x10 (16)	(16, 0)	(16, 0)	(16, 0)	(0, 2)	(1, 2)
0x11 (17)	(17, 0)	(17, 0)	(17, 0)	(2, 2)	(3, 2)
0x12 (18)	(18, 0)	(18, 0)	(18, 0)	(4, 2)	(5, 2)
0x13 (19)	(19, 0)	(19, 0)	(19, 0)	(6, 2)	(7, 2)
0x14 (20)	(20, 0)	(20, 0)	(20, 0)	(8, 2)	(9, 2)
0x15 (21)	(21, 0)	(21, 0)	(21, 0)	(10, 2)	(11, 2)
0x16 (22)	(22, 0)	(22, 0)	(22, 0)	(12, 2)	(13, 2)
0x17 (23)	(23, 0)	(23, 0)	(23, 0)	(14, 2)	(15, 2)
0x18 (24)	—	(0, 1)	(0, 1)	(0, 3)	(1, 3)
0x19 (25)	—	(1, 1)	(1, 1)	(2, 3)	(3, 3)
0x1A (26)	—	(2, 1)	(2, 1)	(4, 3)	(5, 3)
0x1B (27)	—	(3, 1)	(3, 1)	(6, 3)	(7, 3)
0x1C (28)	—	(4, 1)	(4, 1)	(8, 3)	(9, 3)
0x1D (29)	—	(5, 1)	(5, 1)	(10, 3)	(11, 3)
0x1E (30)	—	(6, 1)	(6, 1)	(12, 3)	(13, 3)
0x1F (31)	—	(7, 1)	(7, 1)	(14, 3)	(15, 3)
0x20 (32)	—	(8, 1)	(8, 1)	(0, 4)	(1, 4)
0x21 (33)	—	(9, 1)	(9, 1)	(2, 4)	(3, 4)
0x22 (34)	—	(10, 1)	(10, 1)	(4, 4)	(5, 4)
0x23 (35)	—	(11, 1)	(11, 1)	(6, 4)	(7, 4)
0x24 (36)	—	(12, 1)	(12, 1)	(8, 4)	(9, 4)
0x25 (37)	—	(13, 1)	(13, 1)	(10, 4)	(11, 4)
0x26 (38)	—	(14, 1)	(14, 1)	(12, 4)	(13, 4)
0x27 (39)	—	(15, 1)	(15, 1)	(14, 4)	(15, 4)
0x28 (40)	—	(16, 1)	(16, 1)	(0, 5)	(1, 5)
0x29 (41)	—	(17, 1)	(17, 1)	(2, 5)	(3, 5)
0x2A (42)	—	(18, 1)	(18, 1)	(4, 5)	(5, 5)
0x2B (43)	—	(19, 1)	(19, 1)	(6, 5)	(7, 5)
0x2C (44)	—	(20, 1)	(20, 1)	(8, 5)	(9, 5)
0x2D (45)	—	(21, 1)	(21, 1)	(10, 5)	(11, 5)
0x2E (46)	—	(22, 1)	(22, 1)	(12, 5)	(13, 5)
0x2F (47)	—	(23, 1)	(23, 1)	(14, 5)	(15, 5)

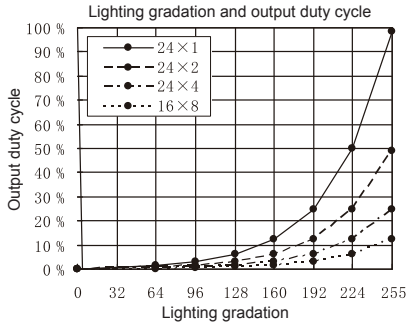
Resistor address	Matrix configuration				
	24×1	24×2	24×4	16×8	
				Even columns	Odd columns
0x30 (48)	—	—	(0, 2)	(0, 6)	(1, 6)
0x31 (49)	—	—	(1, 2)	(2, 6)	(3, 6)
0x32 (50)	—	—	(2, 2)	(4, 6)	(5, 6)
0x33 (51)	—	—	(3, 2)	(6, 6)	(7, 6)
0x34 (52)	—	—	(4, 2)	(8, 6)	(9, 6)
0x35 (53)	—	—	(5, 2)	(10, 6)	(11, 6)
0x36 (54)	—	—	(6, 2)	(12, 6)	(13, 6)
0x37 (55)	—	—	(7, 2)	(14, 6)	(15, 6)
0x38 (56)	—	—	(8, 2)	(0, 7)	(1, 7)
0x39 (57)	—	—	(9, 2)	(2, 7)	(3, 7)
0x3A (58)	—	—	(10, 2)	(4, 7)	(5, 7)
0x3B (59)	—	—	(11, 2)	(6, 7)	(7, 7)
0x3C (60)	—	—	(12, 2)	(8, 7)	(9, 7)
0x3D (61)	—	—	(13, 2)	(10, 7)	(11, 7)
0x3E (62)	—	—	(14, 2)	(12, 7)	(13, 7)
0x3F (63)	—	—	(15, 2)	(14, 7)	(15, 7)
0x40 (64)	—	—	(16, 2)	—	—
0x41 (65)	—	—	(17, 2)	—	—
0x42 (66)	—	—	(18, 2)	—	—
0x43 (67)	—	—	(19, 2)	—	—
0x44 (68)	—	—	(20, 2)	—	—
0x45 (69)	—	—	(21, 2)	—	—
0x46 (70)	—	—	(22, 2)	—	—
0x47 (71)	—	—	(23, 2)	—	—
0x48 (72)	—	—	(0, 3)	—	—
0x49 (73)	—	—	(1, 3)	—	—
0x4A (74)	—	—	(2, 3)	—	—
0x4B (75)	—	—	(3, 3)	—	—
0x4C (76)	—	—	(4, 3)	—	—
0x4D (77)	—	—	(5, 3)	—	—
0x4E (78)	—	—	(6, 3)	—	—
0x4F (79)	—	—	(7, 3)	—	—
0x50 (80)	—	—	(8, 3)	—	—
0x51 (81)	—	—	(9, 3)	—	—
0x52 (82)	—	—	(10, 3)	—	—
0x53 (83)	—	—	(11, 3)	—	—
0x54 (84)	—	—	(12, 3)	—	—
0x55 (85)	—	—	(13, 3)	—	—
0x56 (86)	—	—	(14, 3)	—	—
0x57 (87)	—	—	(15, 3)	—	—
0x58 (88)	—	—	(16, 3)	—	—
0x59 (89)	—	—	(17, 3)	—	—
0x5A (90)	—	—	(18, 3)	—	—
0x5B (91)	—	—	(19, 3)	—	—
0x5C (92)	—	—	(20, 3)	—	—
0x5D (93)	—	—	(21, 3)	—	—
0x5E (94)	—	—	(22, 3)	—	—
0x5F (95)	—	—	(23, 3)	—	—

(Regarding the lighting position and notation)



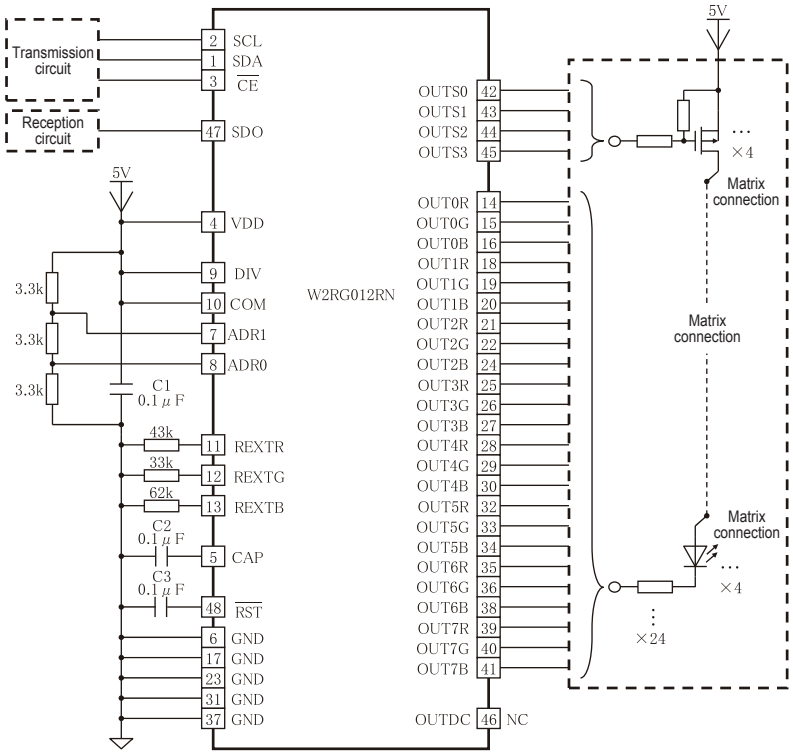
(3, 1) represents the position of ★.

Table 7: Lighting gradation and output duty cycle



Lighting gradation (8 bit) *Representative value	Lighting gradation (7 bit) *Representative value	Lighting gradation (4 bit)	Matrix configuration			
			24×1	24×2	24×4	16×8
0	0	0	(Light off)	(Light off)	(Light off)	(Light off)
15	7	–	0.37 %	0.18 %	0.09 %	0.05 %
31	15	1	0.76 %	0.38 %	0.19 %	0.09 %
47	23	2	1.15 %	0.57 %	0.29 %	0.14 %
63	31	3	1.54 %	0.77 %	0.38 %	0.19 %
79	39	4	2.29 %	1.15 %	0.57 %	0.29 %
95	47	5	3.08 %	1.54 %	0.77 %	0.38 %
111	55	6	4.59 %	2.29 %	1.15 %	0.57 %
127	63	7	6.15 %	3.08 %	1.54 %	0.77 %
143	71	8	9.18 %	4.59 %	2.29 %	1.15 %
159	79	9	12.30 %	6.15 %	3.08 %	1.54 %
175	87	10	18.36 %	9.18 %	4.59 %	2.29 %
191	95	11	24.61 %	12.30 %	6.15 %	3.08 %
207	103	12	36.72 %	18.36 %	9.18 %	4.59 %
223	111	13	49.22 %	24.61 %	12.30 %	6.15 %
239	119	14	73.44 %	36.72 %	18.36 %	9.18 %
255	127	15	98.44 %	49.22 %	24.61 %	12.30 %

■ Application Circuit Example



[Setting example] DIV: 24 x 4 configuration, COM: I2C communication, ADR: device address “1101”, constant current setting R: 59.5 mA (14.9 mA), G: 77.6 mA (19.4 mA), B: 41.3 mA (10.3 mA)
(Values in parentheses are effective values)

■ Precautions for Use

(1) Check the operation at your communication frequency before use.
(2) Each input circuit should be determined with due consideration of the voltage, chattering, and static electricity of the input to be connected.
(3) An electrostatic discharge (ESD) protection circuit is built in, but If static electricity exceeding its function is applied, it may be destroyed. When handling, take sufficient precautions such as grounding your body.
(4) Consider allowable losses under actual operating conditions and perform thermal design with sufficient margins. When the voltage loaded onto the IC is high, such as when the number of LEDs driven in series is small, heat generation in the IC can be reduced by inserting a resistor to distribute power consumption.
(5) This IC has a built-in thermal shutdown circuit. When the chip temperature becomes abnormally high, this circuit operates, the output terminal becomes open, and the chip temperature returns to the normal range. Do not use this circuit as a regular function, as it is an emergency protection function.

OMRON AMUSEMENT Co., Ltd

Regional Contact

Americas
https://components.omron.com/us-en/

Europe
https://components.omron.com/eu-en/

Asia-Pacific
https://components.omron.com/sg-en/

China
https://components.omron.com.cn/

Korea
https://components.omron.com/kr-en/

Japan
https://components.omron.com/jp-ja/

Cat. No. AM-W2-BT-001(E)